Patent claims

1.
An arrangement for inter processor (CPU) or inter computer process signal communication in a system comprising two ore more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or computer communications drivers and driver associated interconnections between the CPUs or computers, characterised in a virtual link handler (VLH) comprising at least one shadow process (SP) for each actual process communicating with at least one actual process resident of another CPU/or computer and a plurality of driver adapters (DA) each communicating with at least one SP and/or an OS.

2.
The arrangement of claim 1, characterised in that a shadow process associated with a CPU or computer of the system is identified by a process identifier (PID) identical to the PID of the actual process associated with another CPU or computer of the system.

3.
The arrangement of claim 1 ~~or 2~~, characterised in that a shadow process identifier (SPID) is assigned to each process.

4.
The arrangement of claim 3, characterised in that the SPID itself is a unique process identifier throughout the system.

5.
The arrangement of claim 3, characterised in that the SPID in conjunction with the processor or computer address is a unique process identifier throughout the system.

6.
The arrangement of ~~any one of the previous claims~~ Claim 1, characterised in that actual processes are statically associated with or residents of particular CPUs or computers of the system.

7.
The arrangement of ~~any one of the previous claims~~ Claim 1, characterised in that the VLH maintains a reference list of the associations of the actual processes with the respective CPUs or computers of the system.

8.
The arrangement of claim 7, characterised in that address tables located at each communicating CPU or computer of the system are developed from the reference list.

9.
The arrangement of ~~any one of the previous claims~~ Claim 1, characterised in that a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporary modified to include at least the PID of the receiving SP.

10.
The arrangement of claim 9, characterised in that a signal communicated from one process on one CPU or computer to another process on another CPU or computer is temporary modified to include the PID of the sending SP.

11.
The arrangement of claim 1, characterised in that the DA of a CPU or computer is provided with an interface to the SPs and/or OS associated with the same CPU or computer.

12.
The arrangement of claim 1 ~~or 11~~, characterised in that the DA of a CPU or computer is provided with an interface to the drivers for CPU or computer interconnections associated with the same CPU or computer.

13.
A method for inter processor (CPU) or inter computer process signal communication in a system comprising two or more CPUs or computers, wherein CPUs or computers include independent operating systems (OS), inter CPU or inter computer communications drivers and driver associated interconnections between the CPUs or computers,

characterised in the steps of:

- transferring on a CPU or computer a signal intended for another process on another CPU or computer from an originating process to a shadow process representing the other process,
- amending parameters of the signal by means of the shadow process and a table including the system address of the other process,
- transferring the amended signal to the other CPU or computer by means of driver adapters, the drivers and the driver associated interconnections,
- receiving the amended signal on the other CPU or computer by a shadow process representing the originating process of the signal,
- amending the received signal by the receiving shadow process by means of parameters carried by the received signal, and
- transferring the amended received signal to the other process for which the signal was intended.